A Neural Stimulator ASIC With an Improved Blocking Capacitor Charge Balancing Method and Speed-Boosting Feedback

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***Abstract*—This paper presents a 16-channel stimulator ASIC for prosthetic sensory feedback that incorporates a compact charge balancing method utilizing an initialization phase to preset the voltage across a series blocking capacitor. The stimulator enforces strict per-cycle charge balance between the total sourced and sunk charge without any residual current, regardless of mismatch between the current sources. To further enhance performance, a speed-boosting feedback loop is introduced to monitor the anodic phase current and temporarily increase the stimulation amplitude, enabling higher stimulation rates. The ASIC was designed and fabricated in a 130-nm BCD CMOS process. For a 1 mA stimulation current, it achieves a 99.96% reduction in unbalanced residual charge compared with a conventional, uncorrected blocking-capacitor-based approach. Incorporating the speed-boosting feedback loop yields a maximum reduction in residual voltage of 21% across pulse rates from 200 Hz to 1 kHz, and a maximum reduction of 30.7% at 200 Hz when the stimulation amplitude is increased from 1 to 4 mA. *In vitro* measurements with electrodes in saline yield a residual voltage of only 1.04 mV, demonstrating the effectiveness of the proposed charge balancing method.**

***Index Terms*—Blocking capacitor, charge balance, integrated circuit, neural stimulation, speed-boosting feedback.**

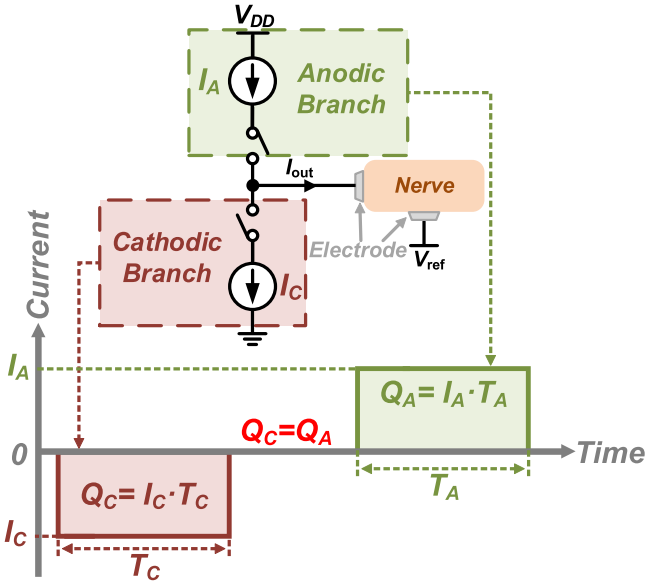

Fig. 1. Operating principle of conventional biphasic stimulation.

I. Introduction

THE lack of meaningful and natural sensory feedback in existing hand prostheses causes more than 30% of prosthesis abandonment [1]. According to recent studies, the most reliable and precise method for interpreting the user's intentions in upper limb prosthetics is through the decoding of muscle electrical activity, while the close-to-natural sensations can be delivered to the human brain by electrically stimulating peripheral nerves [2], [3].

A conventional current mode neural stimulation is shown in Fig. 1. It has a cathodic branch for sinking the current and an anodic branch for sourcing the current. The source and sink currents are injected into the target nerves via electrodes. The stimulation of neurons is achieved by injecting the cathodic current pulse, I_C, into the target nerves. The injected current pulses elicit sensory responses by activating specific neural fibers within the peripheral nerves, enabling the user to perceive sensations such as force, pressure, or slippage. For this particular application, to accommodate variations in nerve fiber recruitment thresholds, the stimulating frequency of the injected current pulses is chosen to be configurable within 1–200 Hz, allowing flexibility for encoding sensory information, while the pulse width (T_C and T_A) is adjustable, typically within 20–300 μs, [3]. The amplitude of the current pulses varies from a few μA to a few mA to suit disparate nerve and electrode interface characteristics. To prevent tissue damage and electrode corrosion caused by charge accumulation, biphasic current pulses are used. During the cathodic phase, the stimulus current, I_C, depolarizes nearby axons to generate the desired sensory information, while the anodic phase neutralizes the accumulated charge on the electrodes utilizing the anodic current, I_A, ensuring safe operation and preventing adverse effects. The total charge sunk in the cathodic phase, Q_C, must ideally equal the total charge sourced in the anodic phase, Q_A, to avoid any residual charge damaging the tissue and electrodes. However, practical implementations have a

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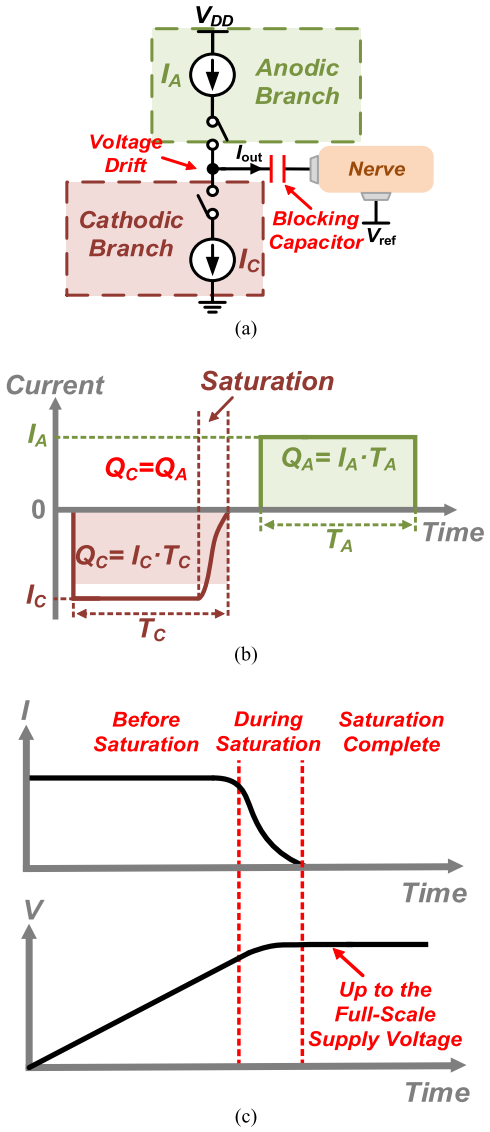

Fig. 2. (a) Simplified block diagram of blocking capacitor-based charge balance method, (b) output current waveform diagram and (c) residual voltage and current during operation.

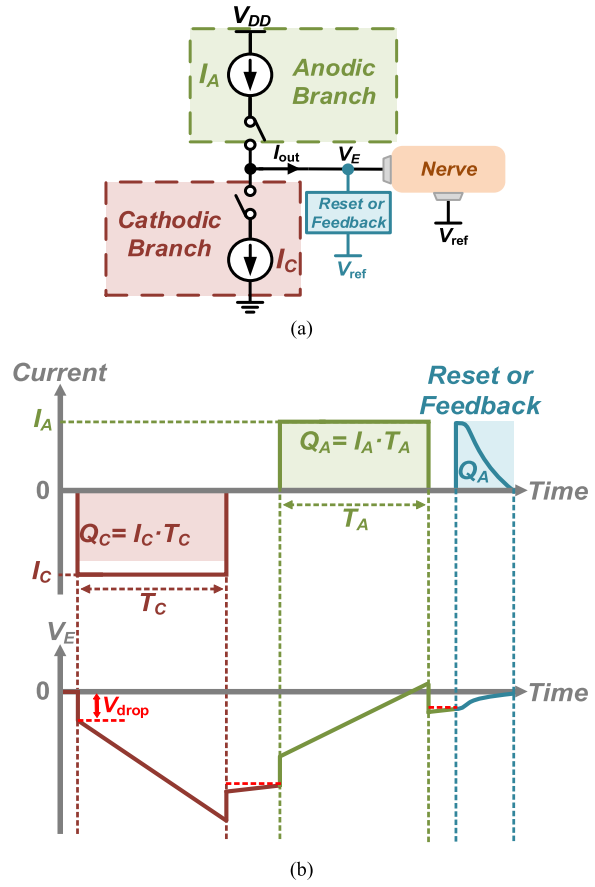

Fig. 3. (a) Simplified block diagram of a stimulator with voltage discharge, and (b) output current and voltage waveforms.

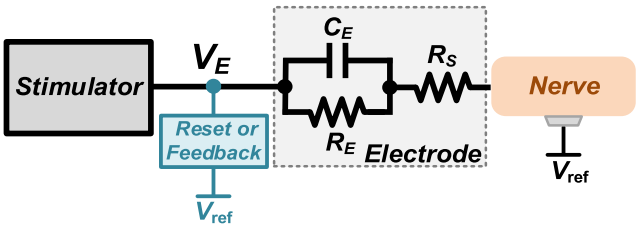

Fig. 4. The neural stimulator system in Fig. 3 with a simplified electrode model.

charge mismatch between the cathodic and anodic phases due to hardware non-idealities. This mismatch leads to an imbalance in the charge delivered causing charge accumulation that compromises the safety performance of the stimulation system.

Various methods have been proposed to address charge accumulation in neural stimulators. The most commonly used solution is to place a blocking capacitor between the electrode and the stimulator, as shown in Fig. 2(a) [4]. This solution effectively protects the tissue and electrode from dc net current. However, an inevitable side effect is that the unbalanced charges due to the mismatch between the cathodic and anodic currents accumulate at the output node of the stimulator, causing a gradual voltage drift. The maximum voltage drift introduced by this process is equal to the mismatch current multiplied by the output impedance of the stimulator (anodic and cathodic current branches). Since current stimulators require large output impedances to deliver the correct charge under various repetitive load conditions, this voltage drift is often sufficient to cause one of the branches to saturate, ultimately resulting in a charge imbalance between Q_C and Q_A, as shown in Fig. 2(b). However, before it is balanced, the unbalanced current charges the load and a maximum residual charge equal to $Q_{MAX} = V \cdot C$ may accumulate at the electrode during this process, where C is the capacitance of the blocking capacitor and V is the supply voltage, as shown in Fig. 2(c). As discussed in [4], [5], and [6] any residual current before dynamic equilibrium is achieved causes a residual voltage at the electrode-capacitor interface, which may potentially damage the electrode and surrounding tissue. An additional effect is that the saturated current further contributes to inaccuracies in the total charge delivered to the nerves, potentially affecting stimulation precision.

Another commonly used method to reduce the impact of unbalanced charge involves directly discharging the accumulated voltage on the electrode. This is typically achieved either by periodically resetting the electrode to a predefined

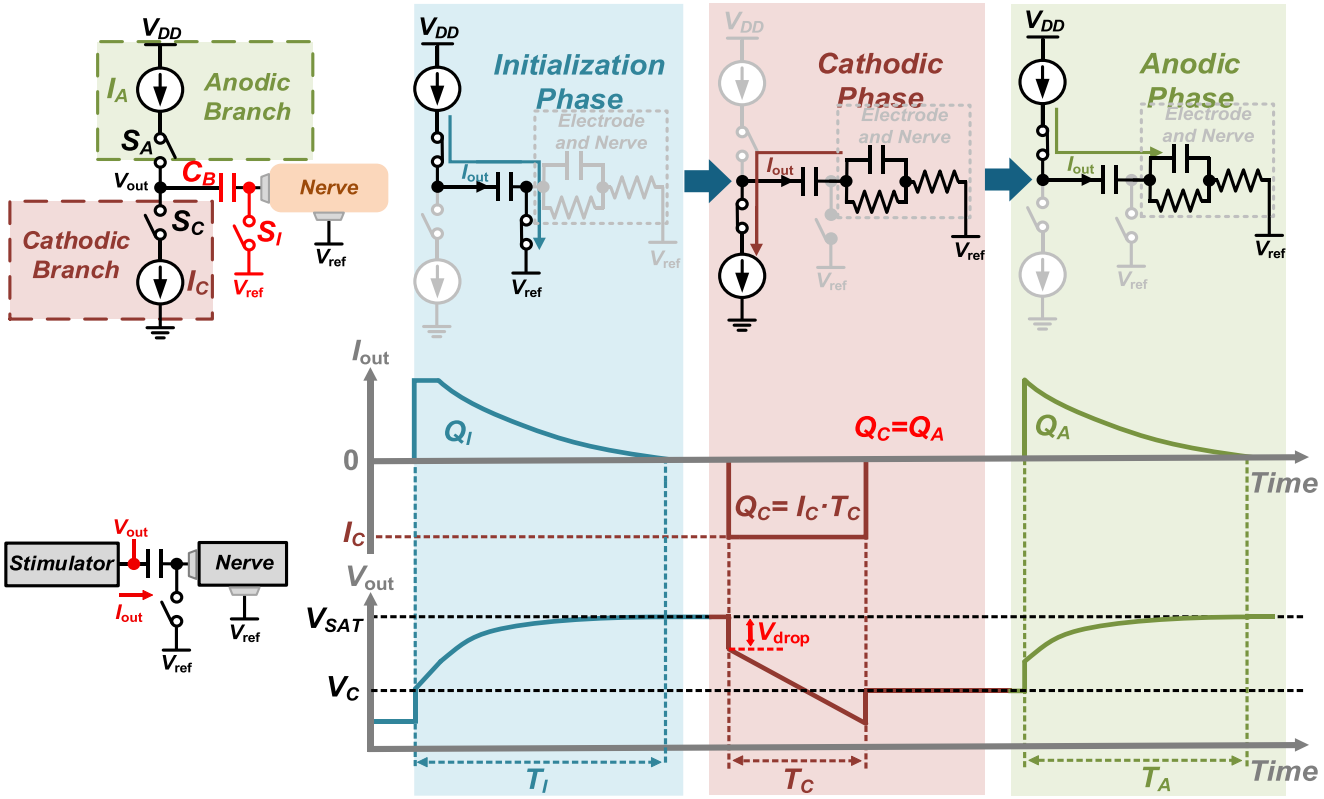

Fig. 5. Simplified block diagram of a stimulator with the proposed charge balancing method and the corresponding I_{out} and V_{out} waveforms at different phases.

common-mode voltage through a switch [4], [5], [6], or by employing a closed-loop feedback system to compensate for the residual voltage, as shown in Fig. 3(a) [7], [8], [9], [10]. Since this method eliminates the need for blocking capacitors, it is well-suited for applications with stringent size constraints, where using blocking capacitors is impractical, such as neural stimulation within the human brain [7]. However, both these methods are based on discharging the residual voltage. A critical issue is that source and sink charges are unequal. During stimulation, the voltage at the electrode, V_E, varies at different times, as shown in Fig. 3(b). The variation of V_E induces a leakage current through the parallel resistor, R_E, as shown in the electrode equivalent model in Fig. 4. Consequently, even if the residual voltage is fully discharged, a total unbalanced residual charge $\Delta Q = \int (V_E/R_E)dt$ is introduced during each stimulation cycle. This continuously unbalanced charge acts as a constant residual dc current and raises serious safety concerns for long-term use, as the persistent dc current drives irreversible Faradaic reactions, accumulates polarization drift, and ultimately degrades tissue safety and electrode longevity [11]. Furthermore, the lack of blocking capacitors compromises the system's fail-safe protection.

To address these challenges, this paper presents a stimulator application specific integrated circuit (ASIC) that employs a novel blocking capacitor charge balancing method. By utilizing an initialization phase that forces the anodic branch into saturation to achieve the same output voltage after each stimulation cycle, this method effectively eliminates the imbalance compared with conventional approaches and achieves a strict charge balance during the entire operation, ensuring enhanced safety and reliability. A speed-boosting feedback loop is further introduced to improve the overall performance. The ASIC was implemented in a 130-nm BCD CMOS process and features 16 stimulating channels. The rest of the paper is structured as follows. Section II explains the principles behind the proposed charge balancing method. Section III presents the circuit design of the stimulator ASIC. Measured results are presented in Section IV. Section V concludes the paper.

II. Proposed Charge Balancing Method

A. Method Overview

To address the imbalance problems, a new blocking capacitor charge balancing method is proposed. The simplified block diagram and the operating sequence are shown in Fig. 5, with the corresponding output voltage V_{out} and current I_{out} waveforms illustrated.

The method introduces an initialization phase before stimulation begins. The anodic switch S_A is turned on, sourcing current to the initialization switch S_I through the blocking capacitor C_B. Because a blocking capacitor is used, there is no dc current path from the stimulator to the nerve, and the output current will charge the output node of the stimulator and drive the output voltage of the stimulator (V_{out}) to its upper limit (V_{SAT}), where the current source in the anodic branch saturates. As the current path in this phase is from the anodic branch to the reference voltage through S_I, the total charge Q_I sourced by the stimulator is discharged via the reference voltage (V_{ref}) while the voltage at the nerve and electrode remains stable.

In the cathodic phase, the cathodic switch S_C is activated while all other switches are turned off, allowing the nerve to be stimulated by the cathodic current. The stimulator's load can be modeled as a capacitor in series with an impedance Z_L. When switch S_C turns on, a sudden voltage drop, V_{drop}, occurs in the output voltage V_{out}, equal to the product of the cathodic current I_C and the load impedance Z_L. Subsequently, V_{out} continues to decrease due to the discharge of the cathodic current through the load. When S_C turns off, the current path from the load is interrupted, causing a sudden voltage rise in V_{out}, equal to V_{drop}. After this, V_{out} stabilizes at a certain voltage V_C. Because before the cathodic phase V_{out} is set to V_{SAT}, the potential saturation issue in the conventional blocking capacitor balance method is avoided, allowing for high precision charge injection to the tissue for neural stimulation. The total charge removed in the cathodic phase is:

$$Q_C = T_C \cdot I_C \tag{1}$$

where T_C is the total time when S_C is on and I_C is the current amplitude of the cathodic current. The total stimulation charge can be easily controlled by adjusting the values of T_C and I_C. The change of V_{out} between its initial voltage V_{SAT} and the final voltage V_C is determined only by the total discharge of the cathodic current Q_C:

$$Q_C = C_B (V_C - V_{SAT}) \tag{2}$$

where C_B is the capacitance of the blocking capacitor.

During the subsequent anodic phase, switch S_C turns off and S_A turns on. Similar to the voltage variation observed in the cathodic phase, there is a step voltage rise equal to the anodic current I_A times the resistive component of the load impedance Z_L in the output voltage V_{out}. Following this initial rise, V_{out} continues to increase due to the charging of the anodic current. Unlike the cathodic current, which has a rectangular waveform, the anodic current decreases exponentially throughout the anodic phase. This behavior is attributed to the fact that the output voltage V_{out} approaches the upper limit voltage V_{SAT}, causing the current source in the anodic branch to operate in the linear region. Sufficient time is allowed in the anodic phase so that the anodic current decreases to very near zero and there is minimal voltage drop when switch S_A turns off. Concurrently, as current I_A decreases to zero, the output voltage V_{out} returns to the upper limit voltage V_{SAT}, where the current source in the anodic branch completely saturates. Hence, the total charge in the anodic phase Q_A is given by:

$$Q_A = C_B (V_{SAT} - V_C) = \int_0^T I_A = |Q_C| . \tag{3}$$

Consequently, the absolute value of charge Q_A in the anodic phase equals charge Q_C in the cathodic phase, and there is no residual charge after a stimulation cycle (one cathodic phase and one anodic phase). This also indicates that the value of Q_A is independent of the value of the anodic current, I_A. For applications requiring enhanced fail-safe operation, an additional blocking capacitor can be added at the shared reference electrode, as shown in Fig. 17(a), to eliminate any potential dc current path in the event of device failure.

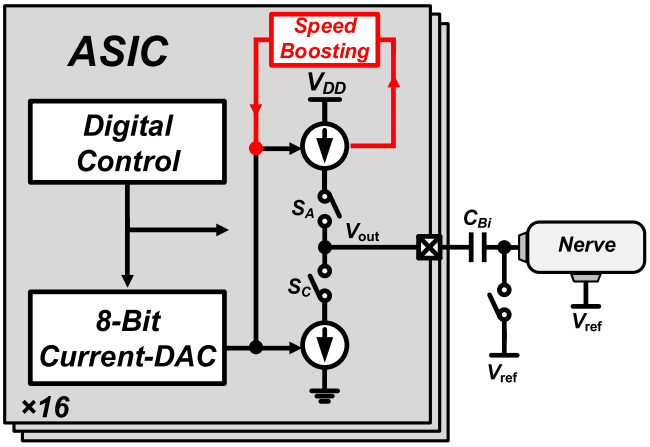

Fig. 6. Simplified block diagram of the stimulator ASIC with the proposed charge balancing method, the speed-boosting feedback, and the added blocking capacitor C_{Bi} to isolate the initialization switch.

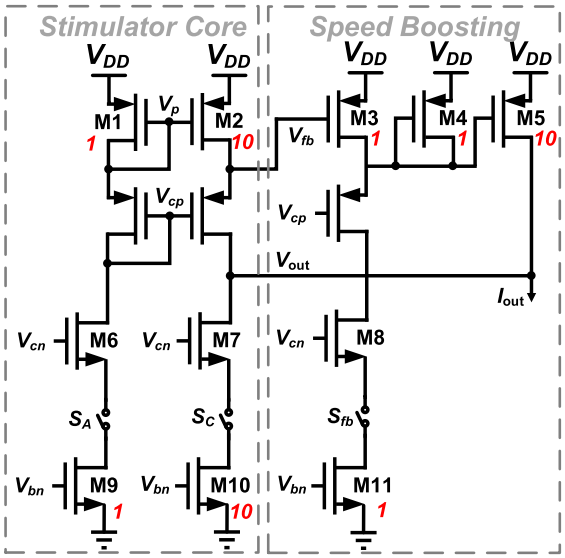

Fig. 7. Schematic of the stimulator core and speed-boosting feedback.

B. Discussion on Discharge Speed and the Residual Voltage and Current

Compared with conventional stimulators with blocking capacitors, the proposed approach effectively eliminates the residual voltage caused by the residual current before dynamic equilibrium is achieved and provides a more precise current stimulation. Because a single initialization phase serves the entire stimulation sequence, sufficient time can be assigned to drive the stimulator output voltage V_{out} to V_{SAT} with no penalty in overall speed. In contrast, the anodic phase repeats each cycle, and its current decays exponentially as V_{out} approaches the supply voltage. Consequently, the settling time required to raise V_{out} close to V_{SAT} becomes a bottleneck that limits the maximum operating frequency and performance of the charge balancing. The voltage displacement introduced by the cathodic phase is given by:

$$V_0 = V_{SAT} - V_C = \frac{Q_C}{C_B} = \frac{T_C \cdot I_C}{C_B} . \tag{4}$$

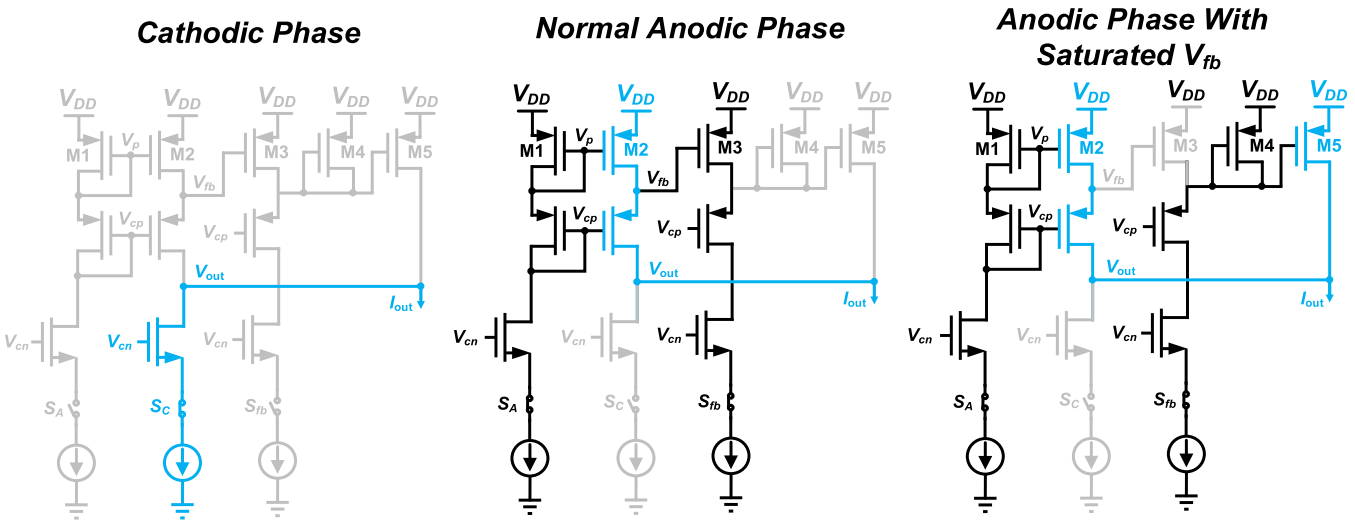

Fig. 8. Operation of the stimulator in cathodic phase, normal anodic phase and anodic phase with speed-boosting feedback engaged.

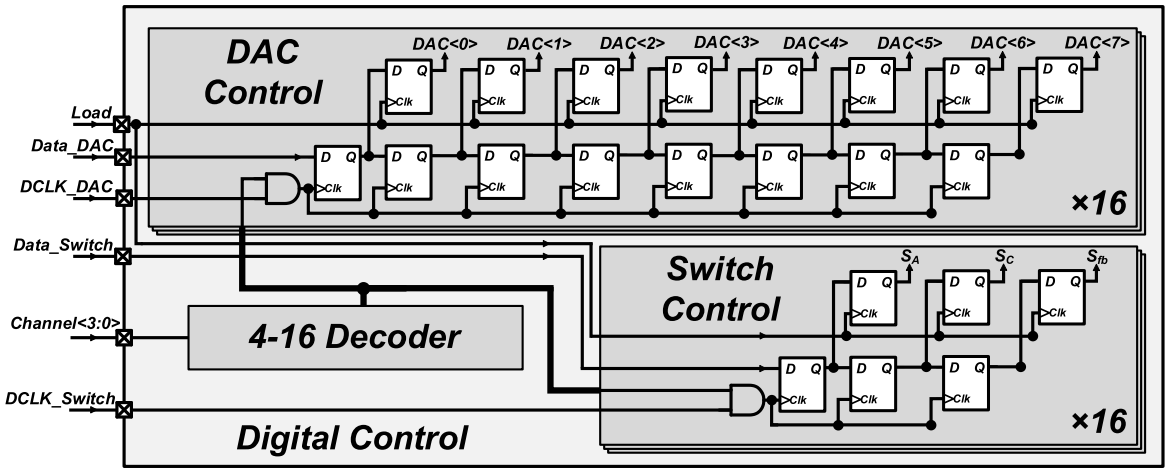

Fig. 9. Schematic of the digital control module with channel selector and shift-register chains.

Given a finite discharge time in the anodic phase, the residual voltage during anodic phase is given by:

$$\Delta V(t) = V_0 e^{-\frac{t}{C_B(Z_E+R_A)}} \tag{5}$$

where $Z_E = R_S + (R_E//C_E)$ is the effective electrode impedance, and R_A is the effective resistance of the anodic discharge branch. This model indicates that the residual voltage is mainly limited by the finite exponential settling during the anodic phase. For a given stimulation charge Q_C, a longer available anodic settling time reduces the residual voltage exponentially, while a larger effective electrode resistance or anodic discharge resistance increases the settling time constant and therefore slows the recovery. In the first order RC model, the blocking capacitor introduces a trade-off: a larger C_B reduces the initial voltage displacement V_0, but also increases the settling time constant. Therefore, the residual voltage is ultimately determined by the combined effect of the initial voltage displacement and the incomplete anodic settling. The electrode capacitance C_E introduces second order impact on the settling speed by affecting the effective resistance in the first order RC model. When the settling-limited component is sufficiently reduced, the ultimate residual floor may be set by other effects such as switch leakage, charge injection and device non-idealities. However, these effects are much smaller than the finite-settling component and do not change the charge balancing principle. It is worth noting that a residual voltage within a safety limit is acceptable for chronically implantable neural stimulators, as can be seen in [7] where a safety window of ±50 mV is suggested.

The exponential recovery characteristic in the anodic phase results in a residual voltage ΔV remaining in a finite time. Similar to conventional blocking-capacitor schemes, this ΔV corresponds to a fixed residual charge $\Delta Q = \Delta V \cdot C$, where C is the blocking capacitor. However, in conventional approaches the residual voltage can approach V_{DD}, whereas in this case ΔV is introduced by insufficient charging; consequently, ΔV is significantly smaller, yielding superior charge balance performance.

In comparison with methods that discharge residual voltage from the electrode (Fig. 3) [4], [5], [6], [7], [8], [9], [10], where the residual voltage resides on the electrode and typically produces a continuous dc residual current that accumulates unbalanced charge over time, the residual voltage in this proposed method is across the blocking capacitor.

Hence the resulting unbalanced charge is a bounded constant value (as discussed above) rather than a time-integrating dc drive, which still exhibits superior charge balance performance.

III. Circuit Design

A. Stimulator ASIC Overview

The block diagram of the stimulator ASIC based on the proposed charge balancing method is shown in Fig. 6. It has 16 independent channels. Each channel comprises a stimulator, an 8-bit current digital-to-analog converter (DAC) and a digital control logic unit. The output current amplitude of the stimulator is defined by the 8-bit current DAC. The digital control logic operates the current DAC and the switches of the stimulator. An additional feedback loop is implemented to boost the speed in the anodic phase.

B. Stimulator Design

The neural stimulator must deliver precise sink and source currents and proper discharge of any accumulated charge. The pulse width, current amplitude and frequency must be programmable to generate different sensory information. The detailed schematic of the neural stimulator is shown in Fig. 7. It has a stimulator core for both current sourcing and sinking, and a speed-boosting feedback loop to increase the discharge speed. The bias current is provided by transistors M9, M10 and M11, with an aspect ratio of 1:10:1. Switch S_A controls the source current in the anodic phase. Switch S_C controls the sink current in the cathodic phase. Switch S_{fb} controls the speed-boosting feedback loop. To increase the output impedance and current accuracy, cascode transistors are implemented at each branch. The bias voltages V_{bn} and V_{cn} are defined by the output current from the current DAC. The three control switches are implemented between the bias current mirror and the cascode transistors to reduce the impact of transient spikes during switching. The stimulator provides current amplitudes from 0 to 4 mA in 256 steps, designed for cuff electrodes. The pulse width and current amplitude are fully programmable through the digital control logic.

C. Speed-Boosting

As discussed in Section II, the charge balance of the proposed method is achieved by initializing the output voltage to the upper limit of the stimulator, V_{SAT}, and the total charge in the blocking capacitor is zero, so that the charges in the cathodic and anodic phases are balanced. However, as the output voltage V_{out} approaches the upper limit V_{SAT}, the current mirror transistor M2 (Fig. 7), runs into its linear region and the discharge current decreases as V_{out} increases, which increases the time required by the anodic phase. A straightforward method is replacing the anodic branch with a switch with small on-resistance. However, the uncontrolled discharge speed of a simple switch would generate a large current spike, potentially impacting system stability and increasing the risk of damaging sensitive circuitry, electrode and tissue [12].

To address this issue, a speed-boosting feedback loop is proposed to increase the discharge speed in the anodic phase while providing a well-controlled discharge current. The operation is shown in Fig. 8. The speed-boosting feedback circuit is implemented to detect the voltage V_{fb} at the drain voltage of M2 in the anodic branch. In the cathodic phase, S_C turns on, and the stimulator sinks current from the load. In the anodic phase, both switches S_A and S_{fb} turn on. When the output voltage V_{out} is far below the upper limit voltage V_{SAT}, transistor M2 provides constant current and linear discharge of the blocking capacitor through the electrodes and nerve. The drain voltage of M2, V_{fb}, equals its gate voltage, V_P. All the current in the speed-boosting feedback branch is sourced by M3, and M4 and M5 are off. When the output voltage V_{out} is close to the upper limit voltage V_{SAT}, the drain voltage, V_{fb}, of M2 is less than its gate voltage and M2 eventually runs into its linear region, reducing the discharge current. As V_{fb} reduces and M2 saturates, M3 turns off and the current in the speed-boosting feedback loop is sourced by M4, and M5 provides discharge current to the load, boosting the discharge speed in both the initialization phase and anodic phase. As the feedback path is gradually activated by the continuous change of V_{fb} when M2 approaches the linear region during the anodic phase, no abrupt low-resistance discharge path is introduced. Therefore, additional overshoot or transient current spikes at the electrode can be avoided. The maximum current during discharge is also limited by the bias current, ensuring safe operation during stimulation. Moreover, under the condition that the anodic phase is sufficiently long to allow complete discharge, the total integrated anodic charge delivered with and without the speed-boosting feedback is the same. Therefore, the dominant stimulation-related energy remains comparable. To limit the additional power overhead introduced by the feedback loop, the aspect ratio between the main anodic branch and the auxiliary feedback branch is set to 10:1.

D. Digital Control

Fig. 9 shows the detailed schematic of the digital control module. It incorporates a 4-to-16 decoder for channel selection, an 8-bit shift-register chain for controlling the current DAC, and a 3-bit shift-register chain for controlling the switches. During operation, the 4-bit channel address is decoded by the 4-to-16 decoder so that only the selected channel is updated. The data for both DAC and switches is written into the shift register chain by the *DCLK* clock signal. When the load signal is triggered, the new data is programmed into that channel, enabling precise and efficient communication across all channels.

In the stimulation protocol used in this work, the channels are addressed sequentially and only the selected channel is activated for stimulation. The stimulation switches of the unselected channels remain off, leaving their output nodes in a high-impedance state. Therefore, the blocking capacitors of inactive channels do not provide a closed current path and do not behave as additional loads to the active channel. Their stored voltages remain approximately unchanged until the corresponding channels are selected again.

IV. Measured Results

A. Chip Overview

The 16-channel stimulator ASIC was designed and fabricated in a 130 nm CMOS technology, with an area of 1.44 mm $\times$1.6 mm. A BCD process with HV transistors

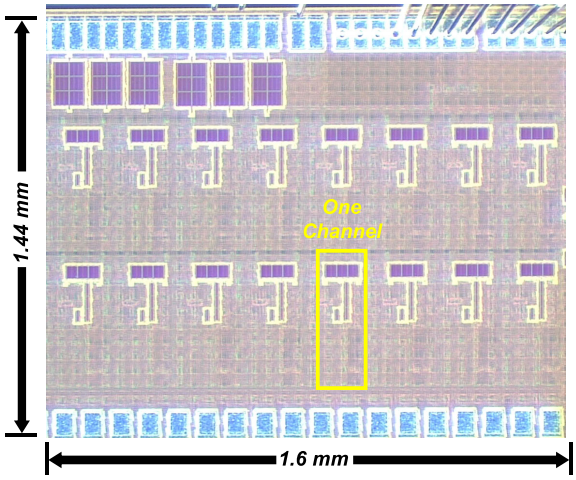

Fig. 10. Micrograph of the 16-channel stimulator ASIC.

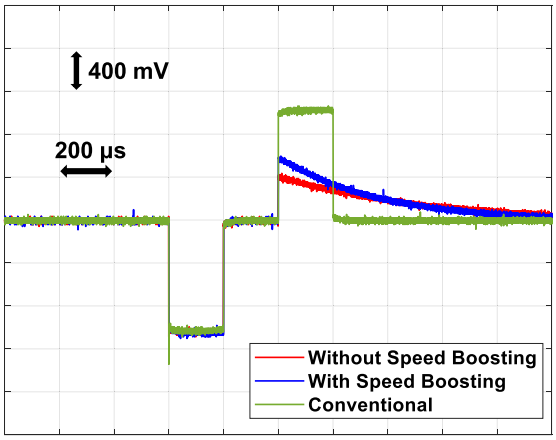

Fig. 11. Output waveforms of stimulators (conventional, with speed-boosting and without speed-boosting) with a 1 kΩ resistive load and 1 mA output current.

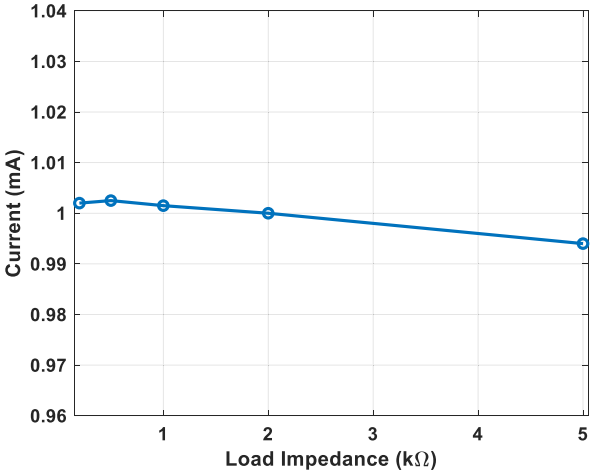

Fig. 12. Output current amplitude of the stimulator in the cathodic phase versus different load impedances.

was used to provide sufficient voltage compliance to drive the electrode and nerve. The chip micrograph is shown in Fig. 10. The output stage of the stimulator operates at 15 V supply and other analog parts at 3.3 V. The digital control module operates

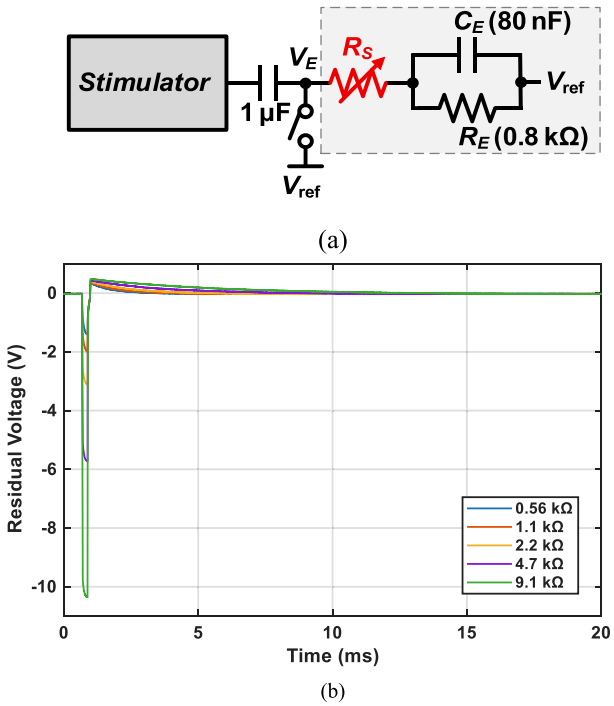

Fig. 13. (a) The experimental setup and (b) the measured residual voltage V_E on the electrode model with different values of R_S.

at 1.2 V. The stimulator ASIC has a quiescent current of 13 μA for all 16 channels in the idle state. Operating at 200 Hz, with 1 mA and 200 μs cathodic pulse width stimulation current, a single channel has a current consumption of 240.1 μA and 141.6 μA, with and without the speed-boosting feedback, respectively.

The output signals were measured on a KEYSIGHT MSOX3024T mixed signal oscilloscope. A CMOD-A7 35T FPGA was used to control the ASIC. A 1 μF off-chip blocking capacitor was used in the measurement. This value was selected to limit the voltage swing across the blocking capacitor under the tested stimulation conditions, with a maximum current amplitude of 4 mA. For applications with smaller stimulation charge or larger allowable voltage swing, the blocking capacitance may be reduced. The initialization switch was implemented by ADG5421 (Analog Devices). A reference voltage of 7.5 V was used.

B. Overall Performance

To evaluate the performance of the stimulator ASIC, a set of resistive loads with different values was used. Fig. 11 illustrates the output waveforms of the stimulator operating at a 1 mA output current with a 1 kΩ resistive load. Initially, the stimulator was tested in a conventional mode, where the speed-boosting feedback loop was disabled, and no specialized charge balancing method was employed. Under these conditions, the output displayed two rectangular pulses, reflecting the baseline operation without enhancements. Subsequently, the stimulator was evaluated using the proposed charge balancing method. With the speed-boosting feedback enabled, the anodic recovery is accelerated. The benefit becomes more pronounced at higher stimulation frequencies and larger stimulation current amplitudes. The slightly higher starting voltage

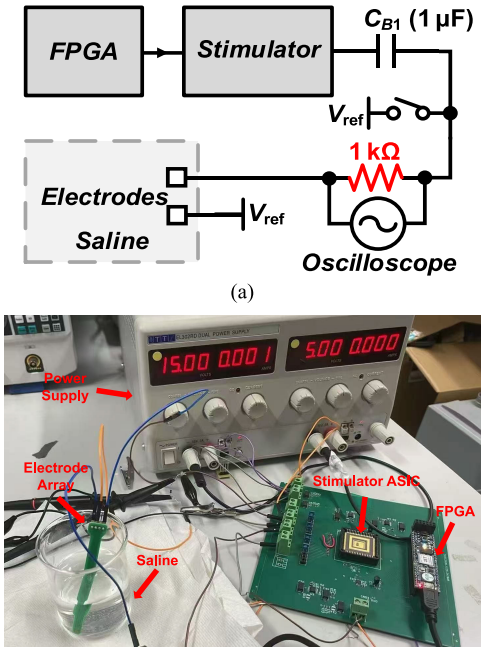

Fig. 14. (a) Block diagram of the test setup with electrodes in saline and (b) photograph of the measurement setup.

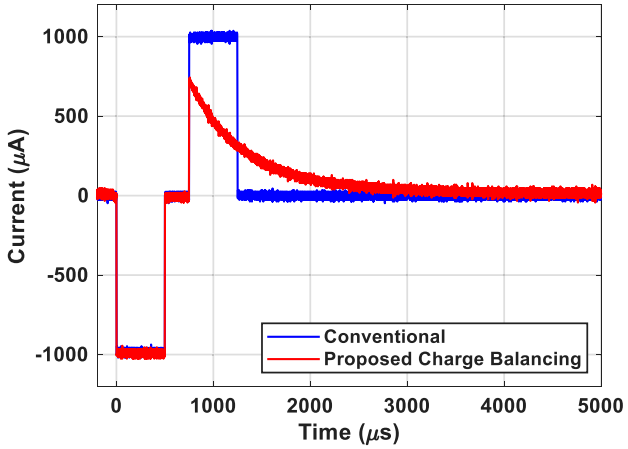

Fig. 15. Saline-test output current waveforms of stimulators with conventional and proposed charge balancing methods.

with speed-boosting is due to the additional anodic current path provided by the feedback branch, which reduces the effective discharge resistance and produces a larger voltage step across the load.

Fig. 12 shows the output current amplitude in the cathodic phase for different load resistances. The load impedance varies from 200 Ω to 5 kΩ. The corresponding output impedance of the stimulator in the cathodic phase is 830 kΩ.

To evaluate the proposed stimulator under different electrode-load conditions, a cuff-electrode model based on [13] was used, with C_E of 80 nF and R_E of 0.8 kΩ (Fig. 13(a)). The series resistance R_S was swept from 560 Ω to 9.1 kΩ to emulate electrode-impedance variations under practical conditions. With 1 mA and 200 µs cathodic stimulation current, the measured residual voltage waveforms are shown in Fig. 13(b).

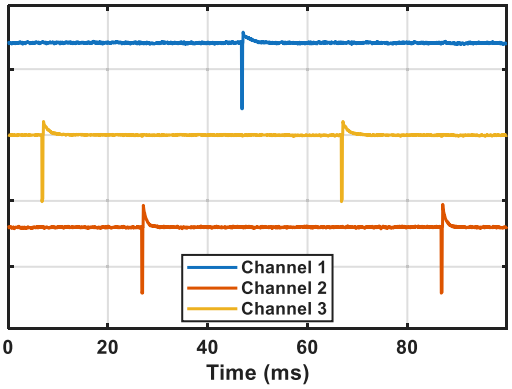

Fig. 16. Measured stimulation current waveforms in multi-channel operation.

As shown in the figure, the residual voltage becomes negligible after a settling time of 15 ms, even under the worst-case condition with 9.1 kΩ R_S resistance, which is much higher than the nominal cuff-electrode load condition considered in this work. To evaluate the impact of channel mismatch on the settling, 10 different channels were tested with 560 Ω R_S resistance, 1 mA and 200 µs cathodic stimulation current at a frequency of 200 Hz. The measured residual voltage from the 10 channels has a mean value of 1.44 mV and a standard deviation of 0.48 mV, with no obvious channel-dependent degradation observed.

C. In-Vitro Tests

To further verify the performance of the stimulator ASIC, it was tested with electrodes in saline with conductivity of 16 mS/cm. A pair of round silver electrodes with a diameter of 0.8 mm was used for stimulation. The pitch between the injecting and return electrodes was 2.27 mm. The electrode has a measured contact impedance of 1.32 kΩ at 1 kHz. A simplified diagram of the test setup is shown in Fig. 14 (a). A 1 kΩ resistor was connected in series with the electrode and the stimulator ASIC to measure the stimulation current. The photograph of the measurement setup is shown in Fig. 14(b). The measured charge balanced current pulses with the conventional and the proposed approach are shown in Fig. 15. The current amplitude of the cathodic phase of both types of current pulse is at 1 mA. To verify the multi-channel operation of the stimulator with the proposed charge balancing method, three stimulation channels were activated sequentially using three electrode channels and a shared return electrode. The measured stimulation current waveforms are shown in Fig. 16. The results confirm that the stimulator can operate sequentially across multiple channels without obvious interference between channels. The peak value of the anodic current varies slightly among channels due to electrode-impedance variation.

D. Charge Balance

As shown in Fig. 2(c), the residual current from the stimulator with blocking capacitors gradually decreases over time and eventually stabilizes at a dynamic equilibrium, where the residual current reaches zero. Consequently, the test setup for residual current in prior work without blocking capacitors [14] is not feasible in this work. A new test setup to evaluate

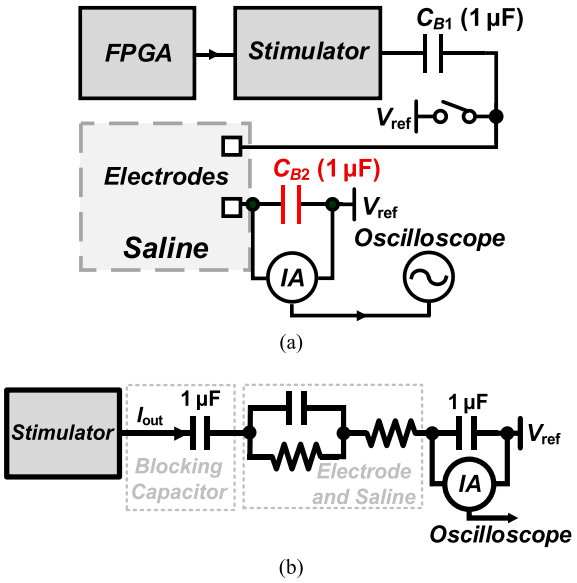

Fig. 17. (a) Block diagram of the test setup for charge balance with an IA for signal recording and (b) the equivalent circuit with a simplified electrode model.

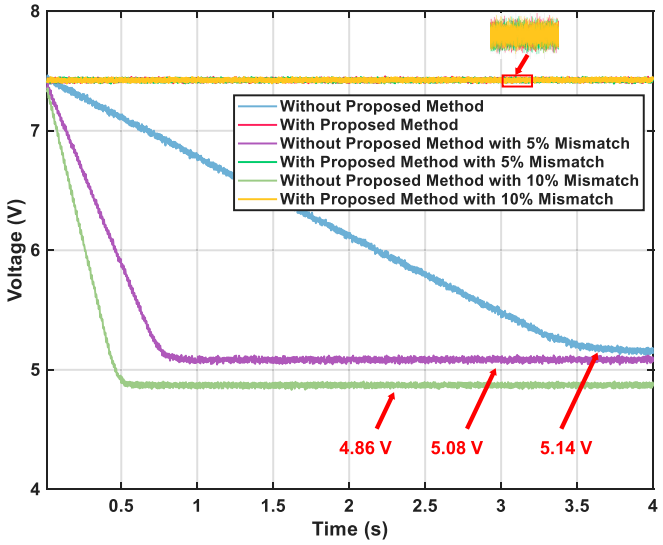

Fig. 18. Measured residual voltage on capacitor C_{B2} for 1 mA, 200 μs pulses at 200 Hz with different cathodic and anodic current mismatches, with and without the proposed charge balancing method.

TABLE I
RESIDUAL VOLTAGES ON ELECTRODE IN SALINE

Injection Current	1 mA	2 mA	3 mA	4 mA
Voltage Difference	0.93 mV	3.95 mV	5.22 mV	7.89 mV

the charge balance performance for stimulators with blocking capacitors is presented in Fig. 17. A capacitor with the same value as the blocking capacitor is placed in series between the return electrode and the reference node. As a result, all the residual current before reaching the dynamic equilibrium is accumulated in this series capacitor and resulting in a variation in its dc voltage. Ideally, the residual voltage on this

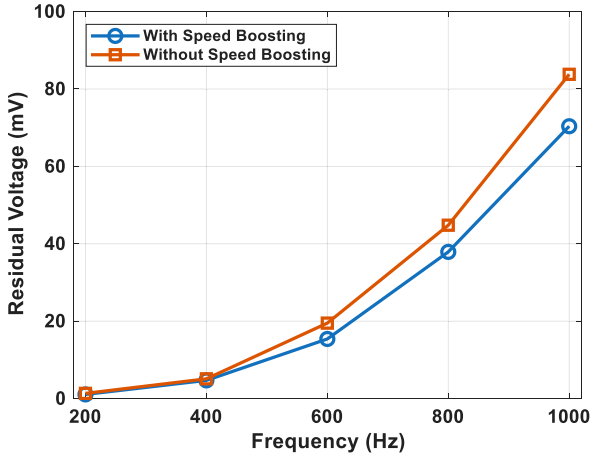

Fig. 19. Measured residual voltage at different stimulation frequencies for 1 mA, 200 μs pulses, with and without speed-boosting.

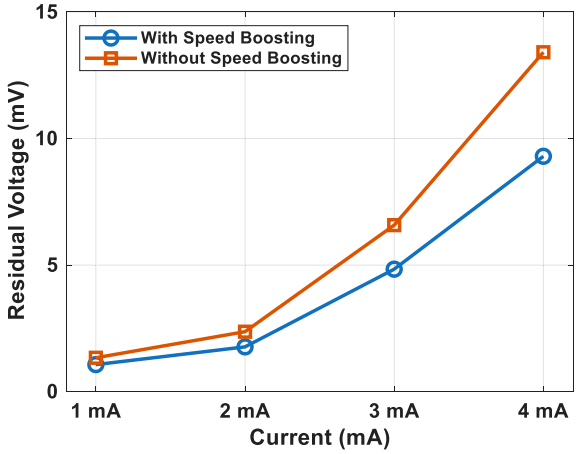

Fig. 20. Measured residual voltage for 200 Hz, 200 μs current pulses at different stimulation current amplitudes, with and without speed-boosting.

capacitor is half of the residual voltage at the output of the stimulator. Measuring the residual voltage on this capacitor directly indicates the performance of the charge balancing and effectively removes any large voltage ripples introduced by the voltage drop across the load during stimulation. To ensure accurate measurement and avoid self-discharge, all the capacitors were MKP4F041005D00KSSD film capacitors with ultra-high insulation. The voltage on the readout capacitor was buffered by an instrumentation amplifier (IA) (OPA2140, Texas Instruments). This provides a minimized leakage current. A 7.5 V voltage reference was used in this test.

Fig. 18 shows a comparison between the measured dc residual voltage (using a moving average filter to extract the dc level variation) on capacitor C_{B2}, with and without the proposed charge balancing method, for 1 mA, 200 μs current pulses at a stimulation frequency of 200 Hz. In addition, 5% and 10% offsets were manually introduced to measure the corresponding voltage variation. Without the proposed method and with no extra mismatch introduced a residual voltage of 2.36 V was obtained. The residual voltage increased to 2.42 V and 2.64 V with 5% and 10 % mismatch respectively. According to the slope of the different waveforms without the proposed charge balancing method, it suggests that the stimulator has around 1% intrinsic mismatch current between

TABLE II
COMPARISON WITH PRIOR WORK

Parameter	[7]	[15]	[16]	[17]	[8]	[18]	[19]	**This work**
CMOS Process (nm)	350	180	180	350	180	180	180	130
Number of Channels/Stimulators	1	1	1	8	16	4	1	16
Stimulating Frequency (Hz)	≤ 100	N/A	< 480	1-100	2-200	N/A	50-500	0-200
I_{max} (mA)	5.12	3	N/A	1.35	12.75	14	N/A	4
Resolution (bit)	9	4	N/A	5	8	8	N/A	8
Voltage Compliance (V)	22	12	5	4	40	20	1.8	15
Charge Balance Precision	±20 mV[a]	6.6 nA	1.9 mV[a]	50 mV[a]	1 nA	2 mV[a]	2.15 %	1.04 mV[b] 1.44±0.48 mV[c]
Static Power/Channel[d] (µW)	31.8	≤ 150	3	100	N/A	N/A	N/A	2.68

[a] Residual voltage on the electrode.
[b] Residual voltage on a 1 µF blocking capacitor at a 1 mA stimulation current in *in vitro* tests.
[c] Residual voltage distribution measured on a RC model across 10 different channels.
[d] Static power consumption when the stimulator is idle.

the anodic phase and cathodic phases. The top horizontal traces (which appear superimposed) represent the proposed method with and without additional mismatch. The magnified section shows a residual voltage of only 1.04 mV, corresponding to a 99.96% reduction in voltage variation compared with a conventional blocking-capacitor approach without correction. In practical biological interfaces, the more complex and time-varying electrode-tissue impedance may increase the residual voltage by reducing the anodic settling margin, but it would not alter the proposed charge balancing mechanism.

Fig. 19 compares the voltage variation with and without the speed-boosting circuit at different stimulation frequencies, with a current amplitude of 1 mA and a pulse width of 200 μs. With speed-boosting, a maximum reduction of 21% in residual voltage is achieved compared with the case without speed-boosting feedback.

Fig. 20 shows the residual voltage as a function of stimulation current amplitude from 1 mA to 4 mA at 200 Hz with a pulse width of 200 μs. A maximum reduction of 30.7% in the residual voltage was achieved using the speed-boosting feedback loop, compared with the case without speed-boosting feedback.

To further evaluate reliability, the voltage differences measured directly between the injecting and return electrodes for stimulation current amplitudes ranging from 1 mA to 4 mA at 200 Hz with a 200 μs pulse width, using the proposed charge balancing method with speed-boosting feedback, are listed in Table I. The measured voltage differences range from 0.93 mV to 7.89 mV.

V. CONCLUSION

This paper has presented a 16-channel stimulator ASIC with a new charge balancing method based on a blocking capacitor. The method reduces residual charge by up to 99.96% compared with conventional blocking-capacitor approaches. A speed-boosting feedback loop has been employed to further improve the performance of the charge balancing method, achieving a maximum reduction in residual voltage of 21% across 200 Hz to 1 kHz and up to 30.7% for current amplitudes from 1 mA to 4 mA at 200 Hz with a 200 μs pulse width. A comparison with prior work is presented in Table II. It shows that this stimulator ASIC achieves the lowest residual voltage reported in the literature.

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